What is claimed is:

1) A phase locked loop circuit, comprising:

a phase-frequency detector capable of providing a phase difference signal responsive to an input signal and a feedback signal;

a charge-pump, coupled to the phase-frequency detector, capable of providing a first voltage responsive to the phase difference signal;

a filter, coupled to the charge-pump, capable of providing a second voltage responsive to the first voltage;

a first voltage-controlled oscillator, coupled to the filter, capable of providing the feedback signal responsive to the second voltage; and,

a second voltage-controlled oscillator, coupled to the filter, capable of providing the feedback signal responsive to the second voltage.

2) The phase locked loop circuit of claim 1, further comprising:

a multiplexer, coupled to the first and second voltage-controlled oscillators, capable of providing the feedback signal responsive to a control signal.

3) The phase locked loop circuit of claim 1, wherein the charge pump includes an adjustable gain responsive to a control signal.

4) The phase locked loop circuit of claim 3, wherein the adjustable gain corresponds to a current.

5) The phase locked loop circuit of claim 1, wherein the filter includes an adjustable resistor responsive to a control signal.

6) The phase locked loop circuit of claim 1, further comprising:

a multiplexer, coupled to the first and second voltage-controlled oscillators, capable of providing the feedback signal responsive to a control signal,

wherein the charge pump includes an adjustable gain responsive to the control signal,

wherein the filter includes an adjustable resistor responsive to the control signal.

7) The phase locked loop circuit of claim 1, further comprising:

a voltage regulator, coupled to the filter and the first and second voltage-controlled oscillators, capable of providing the second voltage.

8) The phase locked loop circuit of claim 7, wherein the voltage regulator includes an operational amplifier.

9) The phase locked loop circuit of claim 1, further comprising:

a phase mixer coupled to the first and second voltage-controlled oscillators.

10) The phase locked loop circuit of claim 1, further comprising:

a clock buffer coupled to the first and second voltage-controlled oscillators.

11) The phase locked loop circuit of claim 1, wherein the filter includes a low-pass filter.

12) The phase locked loop circuit of claim 1, wherein the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit.

13) The phase locked loop circuit of claim 12, wherein the phase locked loop circuit, the serializer circuit and deserializer circuit are included in a memory device.

14) A phase locked loop circuit, comprising:

a phase-frequency detector capable of providing a phase difference signal responsive to an input signal and a feedback signal;

a charge-pump, coupled to the phase-frequency detector, capable of providing a first voltage responsive to the phase difference signal;

a filter, coupled to the charge-pump, capable of providing a second voltage responsive to the first voltage;

an amplifier, coupled to the filter, capable of providing a buffered voltage responsive to the second voltage;

a multiplexer, coupled to the amplifier, capable of providing the buffered voltage responsive to a control signal;

a first voltage-controlled oscillator, coupled to the multiplexer, capable of providing the feedback signal responsive to the buffered voltage; and,

a second voltage-controlled oscillator, coupled to the multiplexer, capable of providing the feedback signal responsive to the buffered voltage.

15) The phase locked loop circuit of claim 14, wherein the charge pump includes an adjustable gain responsive to the control signal.

16) The phase locked loop circuit of claim 15, wherein the adjustable gain corresponds to a current.

17) The phase locked loop circuit of claim 14, wherein the filter includes an adjustable resistor responsive to the control signal.

18) The phase locked loop circuit of claim 14, further comprising:

a phase mixer coupled to the first and second voltage-controlled oscillators.

19) The phase locked loop circuit of claim 14, further comprising:

a clock buffer coupled to the first and second voltage-controlled oscillators.

20) The phase locked loop circuit of claim 14, wherein the filter includes a low-pass filter.

21) The phase locked loop circuit of claim 14, wherein the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit.

22) The phase locked loop circuit of claim 21, wherein the phase locked loop circuit, the serializer circuit and deserializer circuit are included in a memory device.

23) A phase locked loop circuit, comprising:

a phase-frequency detector capable of providing a phase difference signal responsive to an input signal and a feedback signal;

a charge-pump, coupled to the phase-frequency detector, capable of providing a first voltage responsive to the phase difference signal;

a filter, coupled to the charge-pump, capable of providing a second voltage responsive to the first voltage;

a first amplifier, coupled to the filter, capable of providing a first buffered voltage responsive to the second voltage;

a second amplifier, coupled to the filter, capable of providing a second buffered voltage responsive to the second voltage;

a first voltage-controlled oscillator, coupled to the first amplifier, capable of providing the feedback signal responsive to the first buffered voltage; and,

a second voltage-controlled oscillator, coupled to the second amplifier, capable of providing the feedback signal responsive to the second buffered voltage.

24) The phase locked loop circuit of claim 23, wherein the charge pump includes an adjustable gain responsive to a control signal.

25) The phase locked loop circuit of claim 24, wherein the adjustable gain corresponds to a current.

26) The phase locked loop circuit of claim 23, wherein the filter includes an adjustable resistor responsive to a control signal.

27) The phase locked loop circuit of claim 23,

wherein the first amplifier is operational responsive to a control signal,

wherein the second amplifier is operational responsive to the control signal,

wherein the charge pump includes an adjustable gain responsive to the control signal,

wherein the filter includes an adjustable resistor responsive to the control signal.

28) The phase locked loop circuit of claim 23, further comprising:

a phase mixer coupled to the first and second voltage-controlled oscillators.

29) The phase locked loop circuit of claim 23, further comprising:

a clock buffer coupled to the first and second voltage-controlled oscillators.

30) The phase locked loop circuit of claim 23, wherein the filter includes a low-pass filter.

31) A method, comprising:

obtaining a phase difference signal responsive to an input signal and a feedback signal; and,

providing an adjustable frequency range for the feedback signal responsive to a control signal.

32) The method of claim 31, wherein a phase locked loop circuit performs the method.

33) The method of claim 31, wherein the providing includes adjusting a current of a charge pump.

34) The method of claim 31, wherein the providing includes adjusting a resistance in a filter.

35) The method of claim 31, wherein the providing includes selecting an output of a multiplexer.

36) The method of claim 31, wherein the providing includes selecting an operation of an amplifier.

37) The method of claim 31, wherein the providing comprises:
providing a first control signal to a charge pump;
providing a second control signal to a filter; and,
providing a third control signal to a multiplexer.

38) A circuit, comprising:

a phase locked loop circuit capable of providing an output signal responsive to a comparison of an input signal and the output signal; and,

means, coupled to the phase locked loop circuit, for adjusting a frequency range of the output signal responsive to a control signal.